

Course Name : Electronics Engineering Group

Semester : Third

Course Code : EJ/EN/ET/EX/IS/IE/IC/DE/MU IU ED/EI

Subject Title : Principles of Digital Techniques **Subject Code:** 9040

Teaching and Examination Scheme:

Teaching Scheme			Examination Scheme						
TH	TU	PR	Paper	TH	TEST	PR	OR	TW	TOTAL
03	--	02	03	80	20	--	--	25@	125

Rationale:

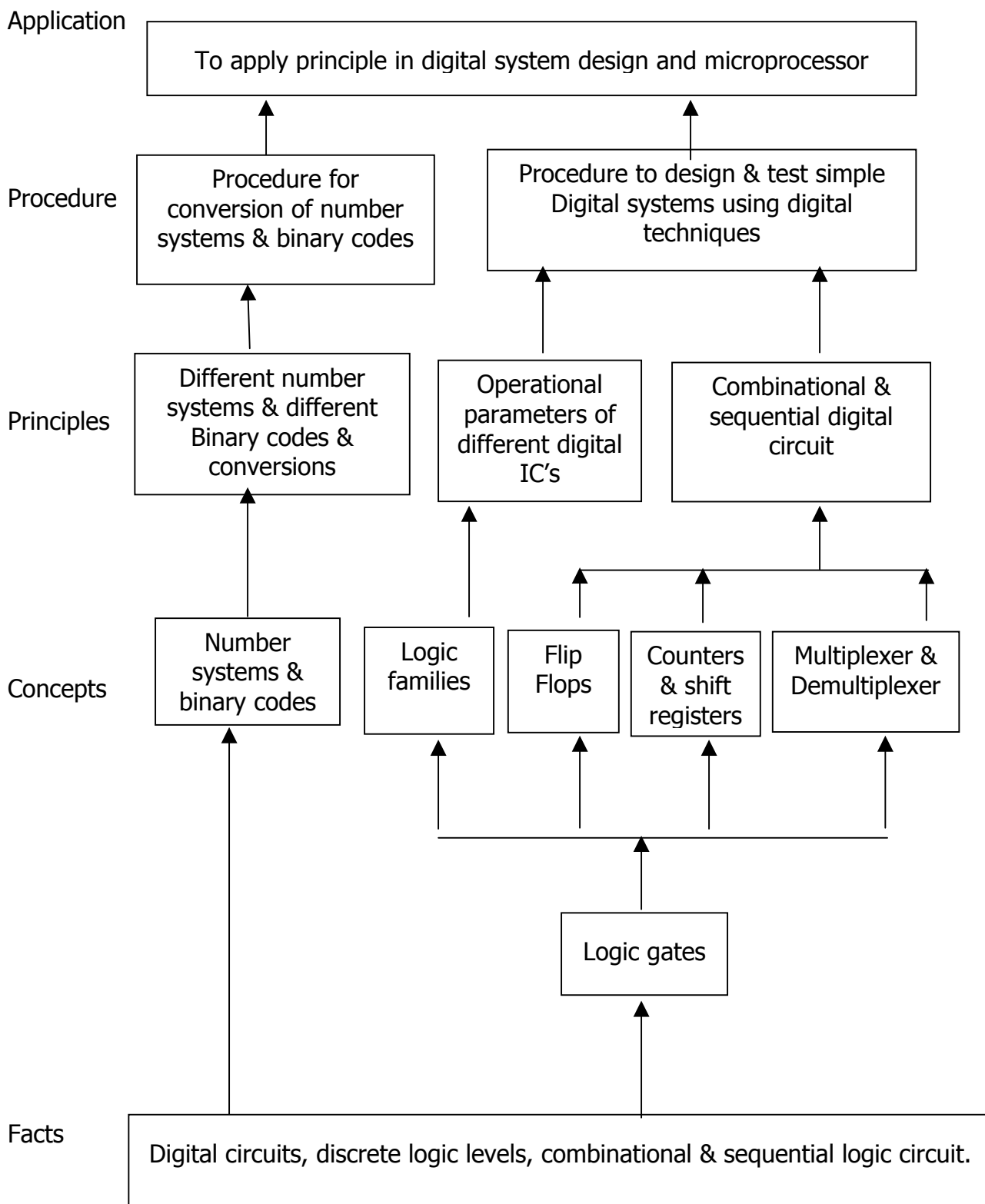
The advancements in microelectronics design, manufacturing, computer technology and information systems have caused the rapid increase in the use of digital circuits. Hence this subject is intended to learn facts, concepts, principles and applications of digital techniques. Thus, students can sharpen their skills of digital design by learning the concept of number systems, logic gates, combinational and sequential logic circuits etc.

Objectives:

The subject student will be able to

1. Design basic digital circuits.
2. Do conversion of number systems.
3. Describe operation of basic logic gates.
4. Design of combinational circuit.
5. Design of sequential circuit.
6. Compare logic families.

Learning Structure:



Contents: Theory

Chapter	Name of the Topic		Hours	Marks
1.	Number System		06	10
	1.1	Introduction to digital system.		
	1.2	Number System - Introduction to Binary, Octal, Decimal, Hexadecimal number system, Conversion of number systems, 1's complement and 2's complement, Binary arithmetic (addition, subtraction, division, multiplication).		
	1.3	Codes - BCD codes, 9's and 10's complement, 8421 BCD codes, Excess – 3 code, gray code, BCD arithmetic (addition, subtraction).		
2.	Logic Gates		04	08
	2.1	Fundamental concepts of Boolean algebra - Basic laws: Cumulative, Complement, Associative, Distributive, De Morgan's theorems.		
	2.2	Logic gates - Basic gates: NOT, AND, OR (Symbol, Truth table, Applications), EX-OR, EX-NOR (Symbol, Truth table, Application), Universal gates: NOR, NAND. NOR as Universal gate, NAND as universal gate.		
3.	Combinational Logic Circuits			
	3.1	Introduction to combinational logic circuit.	10	14
	3.2	Standard representation of Canonical forms (SOP & POS, Minterm, Maxterm) - Conversion between SOP & POS, Numericals based on above topic, Don't care conditions.		

	3.3	K – map reduction techniques and realization (only for SOP – 2, 3, 4 variables), Realization using K – map techniques of Half adder, full adder, Half subtractor, full subtractor, gray to binary, binary to gray converter, BCD to 7 – segment decoder using K-map.		
	3.4	Multiplexer - Necessity of multiplexer, Types of multiplexers 2:1, 4:1, 8:1, 16:1 with realization, Multiplexer Tree, Study of MUX ICs 74150, 74151, 74152, 74153, 74157, Applications of multiplexer.	06	12
	3.5	Demultiplexer - Necessity and Principle of Demultiplexer, Types and realization of De Mux 1:2, 1:4, 1:8, 1:16, Demux Tree, Application of Demux as decoder, Study of ICs 74138, 74139, 74154, 74155.		
4.	Sequential Logic Circuit			
	4.1	Introduction to Sequential Logic Circuit - Difference between combinational and sequential circuit.	07	12
	4.2	Triggering methods (edge & level Trigger).		
	4.3	One bit memory cell - RS latch – using NAND & NOR.		
	4.4	Flip Flops - S R Flip flop, Clocked SR flip flop with preset and clear, Drawbacks of SR Flip flop, Clocked JK Flip flop with preset & clear, Race around condition in JK flip flop, Master slave JK flip flop.		
	4.5	D and T flip flop.		
	4.6	Excitation table of flip flops.	07	10
	4.7	Study of IC 7474 and 7475.		

	4.8	Applications of flip flops - Asynchronous counter: up/down, decade, 3 bit synchronous counter design, ring counter, twisted ring counter with wave forms, 4 bit shift register (SISO, SIPO, PISO, PIPO) with waveforms, Study of IC 7490 (mod – 6, mod – 20).		
5.	Logic Families		08	14
	5.1	Characteristics of logic gates: propagation delay, power dissipation, Fan in, Fan out, current sinking, current sourcing.		
	5.2	TTL logic family - Introduction to TTL logic, Realization of basic gates using TTL logic, TTL NAND gate – Totem pole output, open collector.		
	5.3	ECL logic family - Introduction to ECL logic, ECL OR, NOR gate.		
	5.4	MOS families - Introduction to PMOS, NMOS & CMOS logic, Realization of PMOS inverter, NAND, NOR, Realization of NMOS inverter, NAND, NOR, Realization of CMOS inverter, NAND, NOR.		
	5.5	Comparison of different logic families.		
	5.6	Study of 7400 TTL series / CD 4000 series gate ICs.		
		Total	48	80

Practical:

Skills to be developed:

Intellectual skills:

1. Identification of digital IC's of logic gates. Flip-flops, multiplexer and demultiplexers.
2. Ability to test different digital ICs.
3. Ability to design the combinational and Sequential logic circuits.

Motors skills:

1. Ability to build the circuit.
2. To observe the result and handling the equipments.

List of Practical:

1. Realize basic logic gate using diodes & resistors.
2. Verify De' Morgan's Theorem.
3. Prove NAND and NOR gate as universal gate.
4. Design and realize binary to gray and gray to binary converter using gates.
5. Design Half adder & Full adder / Half subtractor & Full subtractor using Logic gates.
6. Verify operation of ICs 74138, 74154, 74155.
7. Realize and verify RS flip flop using NAND and NOR gate.
8. Realize and verify master slave JK Flip flop using NAND gate.
9. Design IC 7490 for MOD – 6 and MOD – 20 counter.
10. Design asynchronous decade counter.

Mini Projects:

1. Design 1 digit BCD to 7 segment decoder using IC7447.
2. Design 4 bit binary adder/subtractor using IC7483.
3. Design 4 bit synchronous counter using IC7476.
4. Design decade counter using IC7492/93.

Learning Resources:

Books:

Sr. No.	Author	Title	Publisher
1.	R. P. Jain	Modern Digital Electronics	Tata McGraw Hill
2.	Malvino & Leach	Digital Principles & Applications	Tata McGraw Hill

3.	Floyd	Digital Fundamentals	Pearson Education, New Delhi
4.	Malvino	Digital Principles	Tata McGraw Hill
5.	M. Morris Mano	Digital logic and Computer Design	Prentice Hall India (PHI)
6.	M. Morris Mano	Digital logic Design	Prentice Hall India (PHI)